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Integration of Back Calculation Anti Windup and Smith Predictor on PID Controller for Varying Time Delay System with Input Constraint

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Abstract: Proportional Integral Derivative (PID) controller is still the most widely used controller in the industry. However, the presence of varying time delay and input constraint cause PID controller performance to deteriorate and produce unsatisfactory operation. This situation becomes worsening if the varying time delay and input constraint come simultaneously during system operation. To tackle this issue, this paper focuses on the integration of smith predictor and back calculation anti windup on PID controller (PID-BC-SP) towards improving the performance of PID controller due to simultaneous presence of uncertain time delay and input constraint on the system. The designated controller is tested on a first order plus dead time model of glycerin bleaching process plant in order to observe the performance of the controller. Results obtained show that PID-BC-SP produces a better performance and higher robustness as compared to PID, PID to anti windup and PID with smith predictor controllers, whilst handling simultaneous presence of input constraint and varying time delay.

Keywords: Back calculation anti windup; Input constraint; PID controller; Smith predictor; Varying time delay system.

1. INTRODUCTION

Proportional Integral Derivative (PID) controller is very important in control engineering field and it is still the most frequently adopted controllers in industrial operations [1-3]. It is estimated that over 90% of industries utilise PID controller feedback algorithm [4-5]. Therefore any improvement in the methodology design towards improving the PID controller performance will potentially give significant impact on engineering fields and the economic [6]. The popularity of the PID controller over other types of controller obtained from sophisticated techniques is due to its simplicity [5,7]. Apart from that, the combination of all three controller actions which are proportional action, P (present element), integral action, I (past element) and derivative action, D (future element) caused the PID controller to possess the capability of dealing with both transient and steady state response improvement [8-9].

In practice, regulations with a fast response which carried minimal overshoot or no overshoot, and capable to maintain performance along set point is extremely required in industry. This strategy is vital to increase the production rate, energy efficiency, reduce waste, maintain product quality and safety [10]. Unfortunately, in order to provide robust controller performance towards achieving desired response and later maintaining, it is a challenging task due to unfavourable features of the system. These features comprise varying time delay and input constraint. It is well known that varying time delay and input constraint are almost unavoidable in reality. Often, both become the main cause for the deterioration of system performance or even destabilisation of the system [11-16] including system with PID controller [17-22]. Therefore, the present of varying time delay and input constraint should not be neglected during designing a robust PID controller.

For designing a robust PID controller, implementation of smith predictor is the most common way to compensate for the impact of varying time delay [23-26]. On the other hand, the influences of input constraint are prevented through the windup scheme either by a conditional approach or adopting back calculation approaches [27-31]. However, in some cases, the robustness performance for those approaches is not assured because they are designed to tackle issues related to varying time delay and input constraint separately. In practice, both of these aspects; varying time delay and input constraint, will exist synchronously in the system. This factor indicates the design of PID controller that could cope with varying time delay and input constraint simultaneously is extremely necessary for providing robust PID controller performance. This paper integrates smith predictor and PID back calculation anti windup on PID controller (PID-BC-SP) towards improving PID controller performance due to simultaneously present of both varying time delay and input constraint. The designated controller is tested on a glycerin bleaching process plant in order to observe the performance of the controller and also, is compared with standard PID, PID with back calculation anti windup (PID-BC) and PID with smith predictor (PID-SP) controllers to highlight the extent of improvement given by the PID-BC-SP controller.

The remaining parts of this paper are organised as follows. Section 2 describes the integration of smith predictor and back calculation anti windup on PID controller (PID-BC-SP) design. Section 3 describes the experimental results and finally, Section 4 describes the summary of the finding.

2. PID CONTROLLER WITH BACK CALCULATION ANTI WINDUP AND SMITH PREDICTOR (PID-BC-SP)

The structure integration of PID-BC-SP is as illustrated in Figure 1 where K_p, T_i and T_d are proportional gain, integral time and derivative time respectively of PID controller that could be determined using specific formulas described in [32]. T_a is indicated for tracking time constant of back calculation anti windup and its value could be chosen between T_i and T_d [33] or $T_a = \sqrt{T_i T_d}$ [34]. Meanwhile, $G_p(s)$, $G_m(s)$, e^{-Lps} and e^{-Lms} are referred as actual process, smith predictor process model, delay of the actual output and delay of the smith predictor process model respectively. According to [35], the $G_m(s) = G_p(s)$ and $e^{-Lms} = e^{-Lps}$.

3. IMPLEMENTATION AND RESULTS

In this work, the performance of PID-BC-SP is tested on a first order plus dead time (FOPDT) model of glycerin bleaching process described in [36] and the transfer function of actual process of the system is described as follow:

$$G_p(s) = \frac{17.8}{1032s + 1} \tag{1}$$

while

$$e^{-Lps} = e^{-90s} \tag{2}$$

Based on the transfer function and by using Ziegler Nichols (ZN) PID tuning formula, the setup of PID-BC-SP, PID-SP, PID-BC and PID are obtained as shown in Table 1.

During the simulation, the desired set point $R(s)$ is fixed at 85°C and the initial temperature condition is set to 30°C. The experiment has been conducted for 10000 secs with sampling time set to 1 sec. The input constraint of the system has been set to 0 V – 5 V for all experiments. For testing the effect of the varying time delay on the controller, the delay has been varied from 0% (at 90 secs) to the 50% (at 135 secs), 100% (at 180 secs) and 150% (at 225 secs) respectively. For evaluation, the performance of the controller has been analysed based on percentage overshoot and settling time based on 2% band while mean square error (MSE) is used to measure the steady state error, which is taken starting from 3000 secs to 10000 secs.

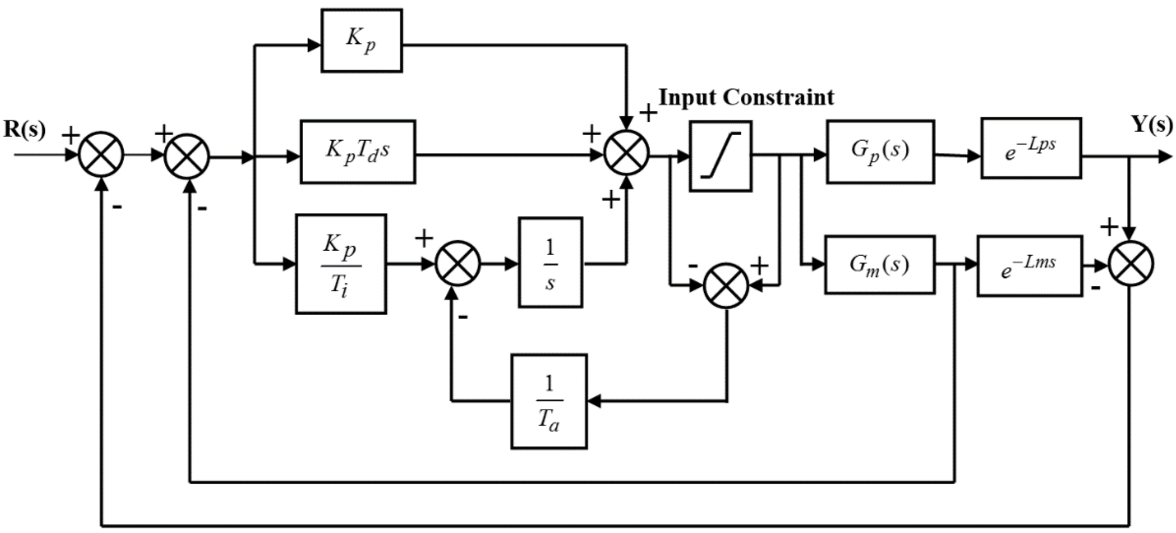

Figure 1. PID with back calculation anti windup and smith predictor (PID-SP-BC) controller structure

Table 1. Controller parameter setup

No	Parameter	Formula	PID-BC-SP Parameter Value	PID-SP Parameter Value	PID-BC Parameter Value	PID Parameter Value
1	K_p	$\frac{1.2\tau}{KL_p}$	0.773	0.773	0.773	0.773
2	T_i	$2L_p$	180	180	180	180
3	T_d	$0.5L_p$	45	45	45	45
4	T_a	$\sqrt{T_i T_d}$	90	-	90	-
5	$G_m(s)$	$G_p(s)$	$\frac{17.8}{1032s+1}$	$\frac{17.8}{1032s+1}$	-	-
6	e^{-Lms}	e^{-Lps}	e^{-90s}	e^{-90s}	-	-

Figures 2-5 show the comparative performance between the PID-BC-SP, PID-BC, PID-SP and PID controllers for the time delays of 90 secs, 135 secs, 180 secs and 225 secs respectively. Meanwhile, the analyses of the controller performance for each of the changes of time delay are as tabulated in Tables 2-5 respectively. The analysis tabulated in Table 2 indicated that the PID-BC-SP is able to compensate the effect of input constraint thus provide a less percentage overshoot and a fast settling time which is 0.6% lower overshoot and 200 secs faster settling time as compared with PID-BC. The analysis on Table 2 also indicated that PID-SP is capable to compensate the effect of input constraint which caused it produces 28% overshoot and require 3905 secs to reach settling time which is 2843 secs slower as compared with PID-BC-SP.

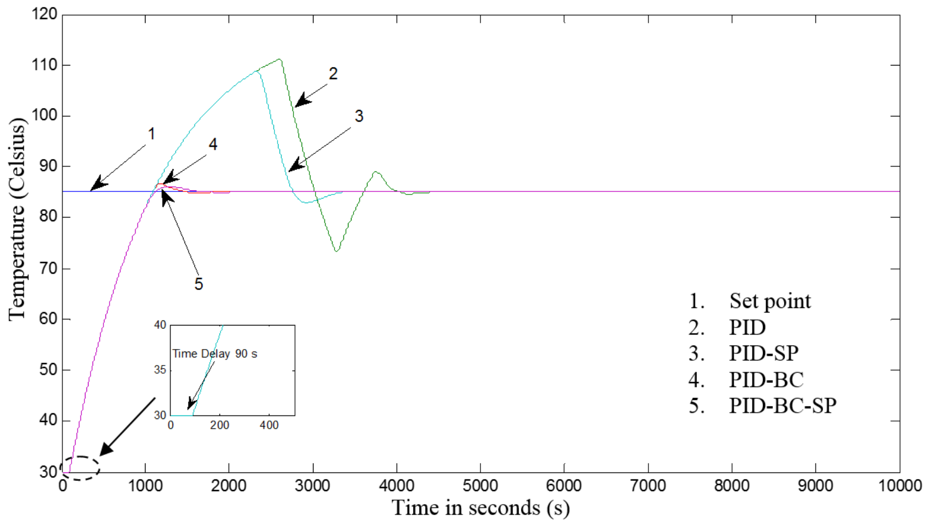

Figure 2. Performance of the controllers with time delay, L_p equal to 90 secs

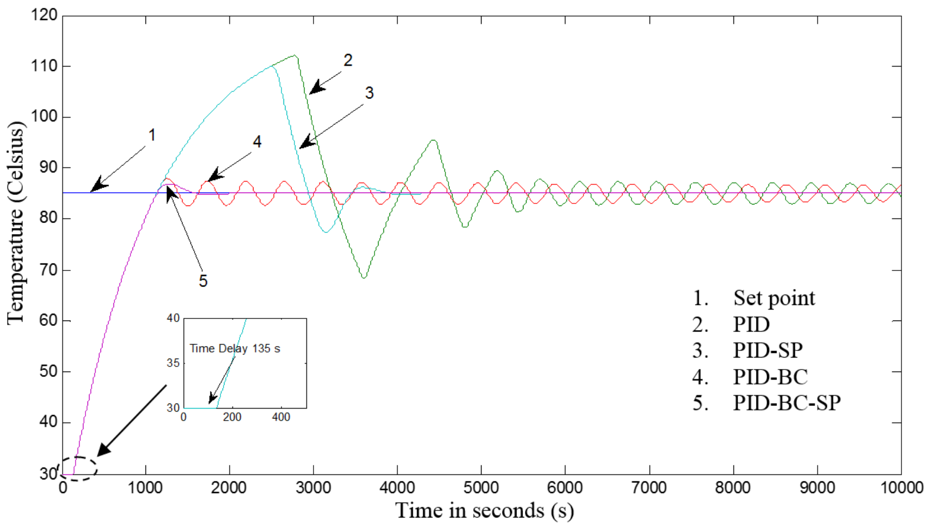

Figure 3. Performance of the controllers with time delay, L_p equal to 135 secs

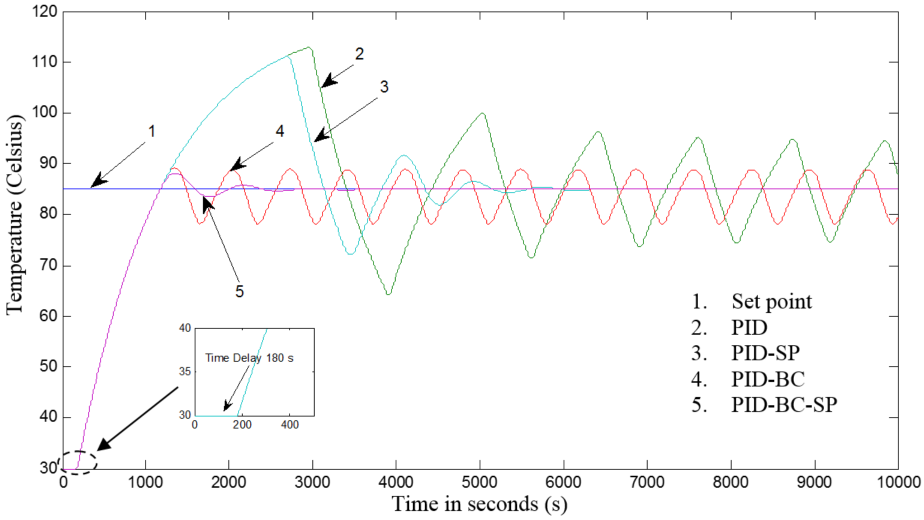

Figure 4. Performance of the controllers with time delay, L_p equal to 180 secs

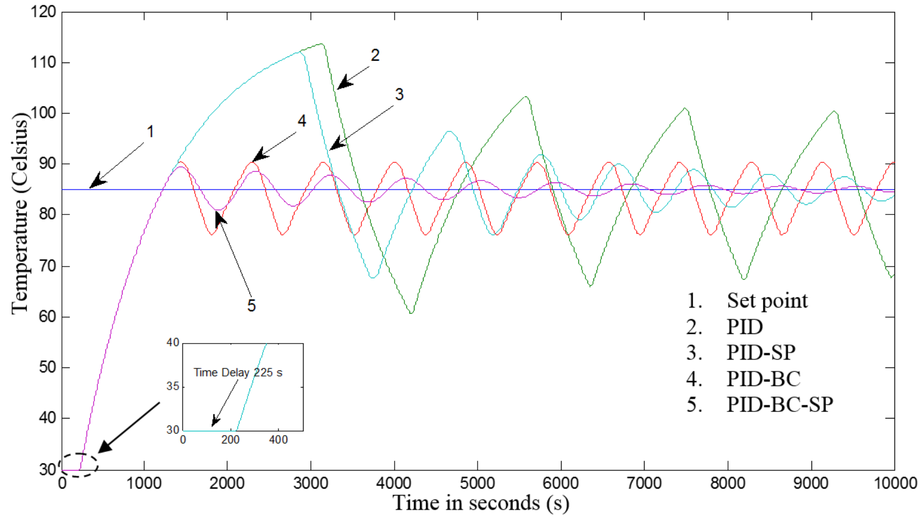

Figure 5. Performance of the controllers with time delay, L_p equal to 225 secs

The performance analysis in Table 3 shows that increment of time delay by 135 secs caused PID and PID-BC to provide oscillating performance. Thus, as an impact, PID and PID-BC controllers are unable to reach settling time along the experimental duration. This situation also occurs to PID and PID-BC controller performance when the time delay is increased to 180 secs and 220 secs as shown in Tables 4 and 5. Besides, the results also indicated that the oscillation magnitude of response produces by PID and PID-BC controller is increased due to the increment of time delay as illustrated in the MSE values shown in Tables 3-5 respectively. These results clearly show that PID and PID-BC controllers are incapable to cope with the time delay increment. The results also indicated these two types of controller are not robust against variation of time delay.

On the other hand, Tables 3 and 4 show that PID-BC-SP and PID-SP are capable to compensate the impact of increasing time delay at 135 secs and 180 secs respectively. This is due to the ability of both controllers in preventing the response from continuous oscillation, thus indirectly be able to achieve the settling time for a given experimental duration. Nevertheless, PID-BC-SP gives a superior performance as compared with PID-SP. This is due to the capability of the PID-BC-SP controller which is able to compensate the simultaneously present of input constraint and varying time delay while PID-SP only capable to compensate varying of time delay. The analysis shown in Table 3 indicated that PID-BC-SP produces only 2.23% overshoot, 1061 secs settling time and $2.89\text{x}10^{-8}$ MSE as compared with PID-SP which produce a response with 29.4% overshoot, settling time at 3904 secs and 1.85 MSE. Meanwhile, Table 4 shows that PID-BC-SP only produced 3.7% overshoot, 1864 secs settling time and $6.57\text{x}10^{-4}$ MSE as compared with PID-SP that produced a response with 30.8%, 5027 secs settling time and 8.86 MSE. From these results, it is clearly indicated that PID-BC-SP provides a better transient and steady state response as compared with PID-SP, when the time delay is increased at 135 secs and 180 secs.

A further increment of time delay to 225 secs caused PID-SP performance to become worst (as depicted in Figure 5). The analysis shown in Table 5 indicated that PID-SP is unable to reach settling time along the experimental duration due to oscillating response. Besides, PID-SP produced 33.8% overshoot and 35.5 MSE. On the other hand, PID-BC-SP achieved its settling time at 9565 secs with 6% overshoot and produces 1.23 MSE. Based on this results it clearly indicated that PID-BC-SP provide a better robustness and performance as compared with PID-SP when time delay increased at 225 secs.

Overall, these results clearly highlight that the PID-BC-SP is capable to compensate the impact of simultaneous presence of input constraint and varying time delay (increment of time delay up to 100%). Besides, the results obtained also reveal that the PID-BC-SP controller provides better robustness performance against simultaneously present of input constraint and varying time delay as compared with PID, PID-BC and PID-SP controllers. Thus, the PID-BC-SP controller is one of the candidates in PID controller design that could be chosen towards improving the performance of PID controller when dealing with the system that possesses varying time delay and input constraint.

Table 2. Analysis performance of the controllers with time delay, L_p equal to 90 secs

Type of controllers	Overshoot (%)	Settling time (s)	MSE
PID	30.8	3905	4.4
PID-BC	1.9	1262	1.2×10^{-11}
PID- SP	28	3126	0.054
PID-BC-SP	1.3	1062	3.03×10^{-9}

Table 3. Analysis performance of the controllers with time delay, L_p equal to 135 secs

Type of controllers	Overshoot (%)	Settling time (s)	MSE
PID	33	unsettle	20.13
PID-BC	1.7	unsettle	1.80
PID- SP	29.5	3905	1.85
PID-BC-SP	2.2	1062	2.89×10^{-8}

Table 4. Analysis performance of the controllers with time delay, L_p equal to 180 secs

Type of controllers	Overshoot (%)	Settling time (s)	MSE
PID	28.3	unsettle	77.36
PID-BC	12.4	unsettle	14.9
PID- SP	30.8	5027	8.86
PID-BC-SP	3.7	1868	6.57×10^{-4}

Table 5. Analysis performance of the controllers with time delay, L_p equal to 225 secs

Type of controllers	Overshoot (%)	Settling time (s)	MSE
PID	66.4	unsettle	154.4
PID-BC	6.4	unsettle	24
PID- SP	33.7	unsettle	35.5
PID-BC-SP	5.9	9566	1.23

4. CONCLUSION

This paper has presented the integration of back calculation anti windup and smith predictor on the PID controller (PID-BC-SP) to improve the performance of PID due to the simultaneous occurrence of input constraint and varying time delay. To evaluate the controller performance, the controller has been tested on temperature regulation of glycerin bleaching process. The simulation results have indicated that PID-BC-SP controller is capable to cope with the simultaneous occasion of input constraint and varying time delay. Concerning on the time delay varying impact, results obtained indicated that PID-BC-SP is capable to cope up to 100% increment in the time delay of the system. Besides, the comparative study between several types of controllers namely, PID-BC-SP with PID controller, PID controller with back calculation anti windup (PID-BC) and PID controller with smith predictor (PID-SP) has indicated that PID-BC-SP provides better performance and robustness against the concurrent emergence of input constraint and varying time delay. This finding demonstrates that PID-BC-SP controller offers another option in PID controller design. It could improve the performance of the PID controller whilst dealing with varying time delay and input constraint possess by the system.

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