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Device-Circuit Level Simulation Study of Three Inputs Complex Logic Gate Designed Using Nano-MOSFETs

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Abstract: Simulation study on silicon-based nano-MOSFETs logic circuits is needed to add more knowledge on the nanoscale circuit performance. Therefore, in this paper, simulation study is carried out on three inputs complex logic gate transistor circuits with four different logic families, namely (i) nano-CMOS complex gate, (ii) nano-MOSFET loaded n-type nano-MOSFET complex gate, (iii) resistive loaded 733.8 Ω nano-MOSFET complex gate, and (iv) pseudo n-type nano-MOSFET complex gate. NanoMOS is used to perform device simulation whereas WinSpice is used to perform circuit simulation. The difficulty faced during downscaling of nano-MOSFET is the realisation of low power high speed nano-MOSFET logic circuits design. Simulation output timing waveforms are used to analyse the timing characteristics of these complex logic circuits with Boolean expression $\overline{\boldsymbol{x}(\boldsymbol{y}+\boldsymbol{z})}$. Transient analysis on nano-MOSFET loaded n-type nano-MOSFET complex gate shows that theoretical modelling calculation of propagation delay and simulated propagation delay is 80% matched. With 10 nm nano-MOSFET complex logic circuits design, dynamic power reduction of 498 times and propagation delay improvement of 20 times are achieved when compared with a typical 120 nm MOSFET logic circuit.

Keywords: Complex gate; Logic family; Nano-MOSFET; Simulation; Theory.

1. INTRODUCTION

Downscaling of MOSFET structural dimensions from micrometer regime to nanometer regime has progressed rapidly over the last few decades [1-8]. Simulation study of 4 nm MOSFET device is available in [9]. However, this simulation used Hafnium Oxide (HfO_2) as oxide material and indium gallium arsenide (InGaAs) as semiconductor material. To use the matured and fully developed Si-based process technology, 10 nm Si-based nano-MOSFET is chosen in this study [10-12]. Four different logic families, namely (i) nano-CMOS complex gate, (ii) nano-MOSFET loaded n-type nano-MOSFET complex gate, (iii) resistive loaded 733.8 Ω nano-MOSFET complex gate, and (iv) pseudo n-type nano-MOSFET complex gate with Boolean function $\overline{x(y+z)}$ have been simulated in this paper. Circuit (i) has NMOS with a channel width, W = 125 nm and a channel length, L = 10 nm whereas PMOS with W = 250 nm and L = 10 nm in order to counter-balance the difference in electron and hole mobility. Circuit (ii) has NMOS with W = 250 nm and L = 10 nm whereas PMOS load with W = 125 nm and L = 10 nm. Circuit (iii) has NMOS with W = 250 nm and L = 10 nm whereas resistance load is 733.8 Ω. Circuit (iv) has NMOS with W = 250 nm and L = 10 nm whereas PMOS with W = 125 nm and L = 10 nm. A constant field scaling technique has been used to scale device dimensions and voltages [13]. Power dissipation and timing characteristics, such as rise time, fall time, maximum operating frequency and propagation delay, are analysed and compared against other research work [14-18]. In Kousik report [19], the benchmarked MOSFET has a structural design of W = 1 μm, L = 120 nm, T_{Si} = 60 nm and V_{DD} = 2.0 V.

2. METHODOLOGY

Device simulation is carried out by using on-line simulator NanoMOS developed by Purdue University. Then, the CIR Spice code files for four different logic circuit families with three inputs complex logic circuits are simulated using WinSpice. The input timing diagrams and output timing diagrams are the output results of WinSpice simulation. To test the three inputs complex logic gates operations with Boolean function $\overline{x(y+z)}$, three inputs signals with periods of 20 ns, 40 ns and 60 ns are considered. The input signals are also used to analyse transient response including rise time, fall time, propagation delay and maximum operating frequency.

2.1 Theory

By using on-line device simulator NanoMOS, the nano-MOSFET device parameters (refer to Table 1) and current-voltage (I-V) graphs (refer to Figure 1 and Figure 2) are obtained which are used to calculate the timing response for nano-MOSFET

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loaded nano-MOSFET complex logical circuit (refer to Table 2) [20]. The truth table for complex logical Boolean function $\overline{x(y+z)}$ is shown in Table 3.

Table 1. Structural dimension of nano-MOSFET

Double Gate Nano-MOSFET Device Simulation Parameters	
V_{GS}	0.60 V
V_{DS}	0.60 V
V_{th}	0.20 V
Source/drain doping concentration (N_D)	1×10^{20} cm^{-3}
Channel body acceptor impurity concentration (N_A)	1×10^{16} cm^{-3}
Channel width (W)	125 nm
Channel length (L)	10 nm
Source length/drain length (L_{SD})	7.5 nm
Silicon channel thickness (T_{Si})	1.5 nm
Top/bottom oxide insulator thickness (T_{OX})	1.5 nm
Top/bottom insulator relative dielectric constant	3.9
Channel body relative dielectric constant	11.7
Top/bottom gate contact work function	4.188 eV

Table 2. Theoretical modelling calculation values of nano-MOSFET loaded nano-MOSFET complex gate

Double Gate Nano-MOSFET Loaded Complex Gate	
Gate capacitance (C_G)	5.755×10^{-17} F
Area capacitance (C_A)	1.612×10^{-19} F
Sidewall capacitance (C_{SW})	6.072×10^{-17} F
Total drain capacitance (C_D)	4.604×10^{-18} F
Total source capacitance (C_S)	1.046×10^{-17} F
Nano-MOSFET loaded resistance (R_{Load})	733.8 Ω
Nano-MOSFET on-state resistance (R_{on})	36.2 Ω
Loaded combinational gate total capacitance at output node (C_{total})	1.335×10^{-16} F
Total capacitance between two nano-MOSFETs connection (C_{SD})	1.967×10^{-17} F
Rise time constant (τ_r)	9.796×10^{-14} s
Rise time (t_r)	1.314×10^{-12} s
Fall time constant (τ_f)	1.803×10^{-15} s
Fall time (t_f)	3.967×10^{-15} s
Propagation delay (t_p)	3.457×10^{-14} s
Maximum signal frequency (f_{max})	7.583×10^{11} Hz

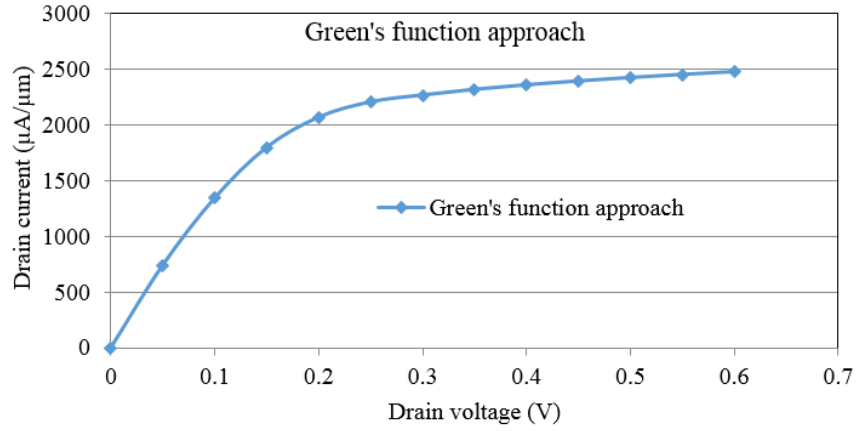


Figure 1. Drain current – drain voltage curve of nano-MOSFET with V_{GS} = 0.60 V

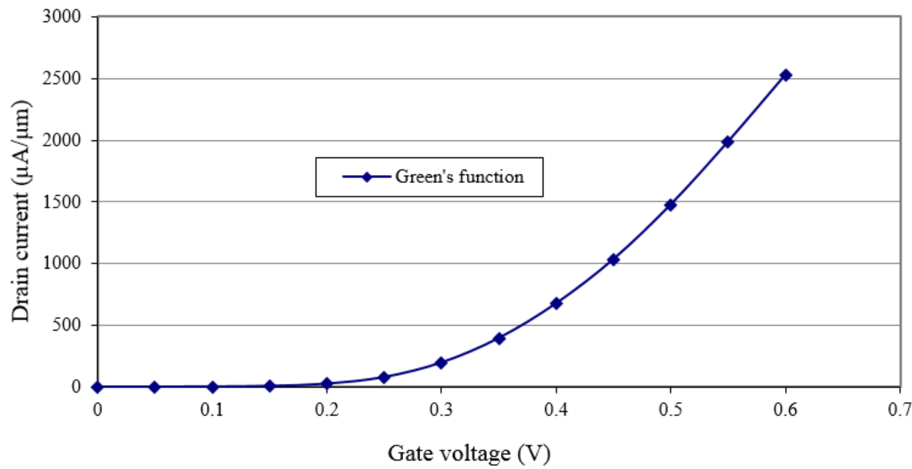


Figure 2. Drain current – gate voltage curve of nano-MOSFET with V_{DS} = 0.60 V

Table 3. Truth table for complex logic gate

Inputs			Output
x	y	z	$\overline{x(y+z)}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Equations and theories, which are used to obtain data in Table 2 are listed below. The drain current per micro width is given by

$$\frac{I_D}{W} = BC_{OX}\widetilde{v_T}(V_{GS} - V_T)\left[\frac{1-\frac{\mathcal{F}_{1/2}\left(\eta_{F1}-\frac{qV_D}{k_BT}\right)}{\mathcal{F}_{1/2}(\eta_{F1})}}{1+\frac{\mathcal{F}_0\left(\eta_{F1}-\frac{qV_D}{k_BT}\right)}{\mathcal{F}_0(\eta_{F1})}}\right] \quad (1)$$

where B is the ballistic efficiency, C_{OX} is the oxide capacitance per unit area, $\widetilde{v_T}$ is the thermal velocity and Fermi-Dirac integrals of order zero and 1/2 are used. All nano-MOSFETs, except for load transistor in nano-MOSFET loaded n-type nano-MOSFET complex gate which operated in resistive region, worked in saturation region with conditions $V_{GS} > V_T$ and $V_{DS} > V_{GS} - V_T$.

$$R_{Load} = \frac{V_{th}}{I_{on-state\ at\ linear\ region} \times W} \quad (2)$$

Since digital logic gates operate at linear portion of I-V curve,

$$R_{channel\ at\ on-state} = \frac{1}{\mu_n C_{OX}(V_{DD}-V_{th})} \tag{3}$$

where $\mu_n = 1200$ cm^2/Vs is the electron mobility at ballistic.

Total capacitance at output node in complex logic (C_{total}) = Gate capacitance + Area capacitance + Sidewall capacitance + (1 × Drain capacitance) + Source capacitance

$$\tau_r = R_{Load} \times \text{Complex gate total capacitance} \tag{4}$$

$$t_r = 2.2 \times \tau_r \times 6.1 \tag{5}$$

It takes 6.1 times duration to pass logic 1 than logic 0 through a n-channel MOS pass transistor. The worst case fall time occurs when x ON, and y or z ON.

$$\tau_f = R_{on}C_n + 2R_{on}C_{out} \tag{7}$$

With the source capacitance, C_{Load},

$$C_{out} = C_{Load} + C_{Dn} = \text{Source Capacitance} + \text{Drain Capacitance} \tag{8}$$

$$C_n = 2C_{Dn} + C_{Sn} = (2\ \times\ \text{Drain Capacitance}) + \text{Source Capacitance} \tag{9}$$

$$\begin{aligned}\tau_f &= R_{on}\big((2 \times \text{Drain Capacitance}) + \text{Source Capacitance}\big) + 2R_{on}(\text{Source Capacitance} + \text{Drain Capacitance}) \\ &= 4R_{on}(\text{Drain Capacitance}) + 3R_{on}(\text{Source Capacitance})\end{aligned} \tag{10}$$

$$t_f = 2.2 \times \tau_f \tag{11}$$

$$t_p = 0.35(\tau_r + \tau_f) \tag{12}$$

$$f_{max} = 1/(t_r + t_f) \tag{13}$$

The theoretical calculated value of output low voltage, V_{OL} of nano-MOSFET loaded n-type nano-MOSFET complex logic gate is given by:

$$V_{OL} = \frac{(2 \times R_{Channel\ at\ on-state})}{(2 \times R_{Channel\ at\ on-state}) + R_{Load}} \times V_{DD} \tag{14}$$

The equation used to obtain dynamic power is

$$P = aCfV_{DD}^2 \tag{15}$$

where a is the activity coefficient, C is the capacitance at output node, f is the frequency of switching and V_{DD} is the voltage supply [21-23].

3. RESULTS AND DISCUSSION

Modern nano-MOSFET devices operate between the drift-diffusion and ballistic regimes. In this paper, quasi-ballistic transport is examined. Figures 3-6 show the schematic circuits of all four logic families of complex logic circuits with Boolean function $\overline{x(y + z)}$.

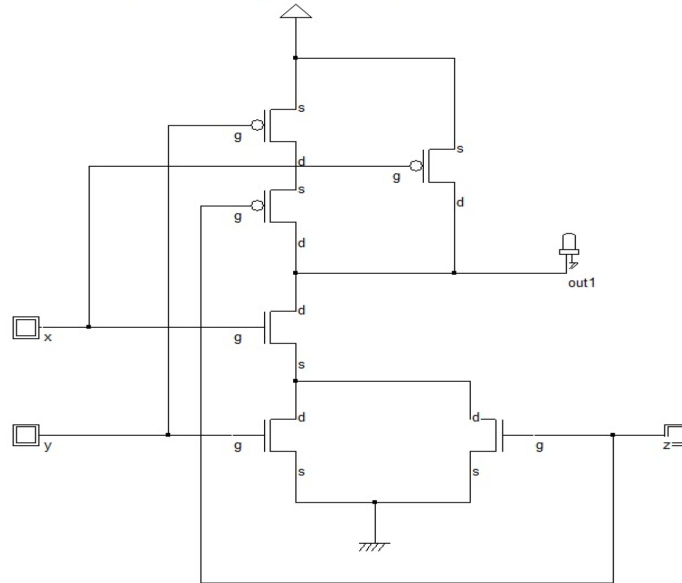


Figure 3. Three inputs nano-CMOS complex logic circuit

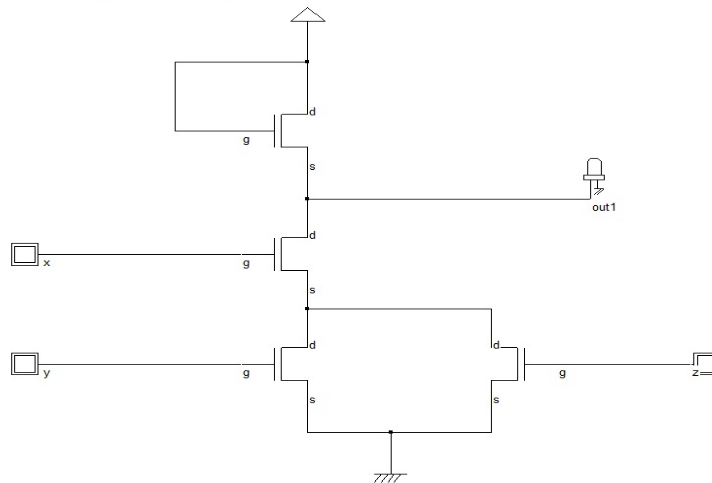


Figure 4. Three inputs nano-MOSFET loaded n-type nano-MOSFET complex logic circuit

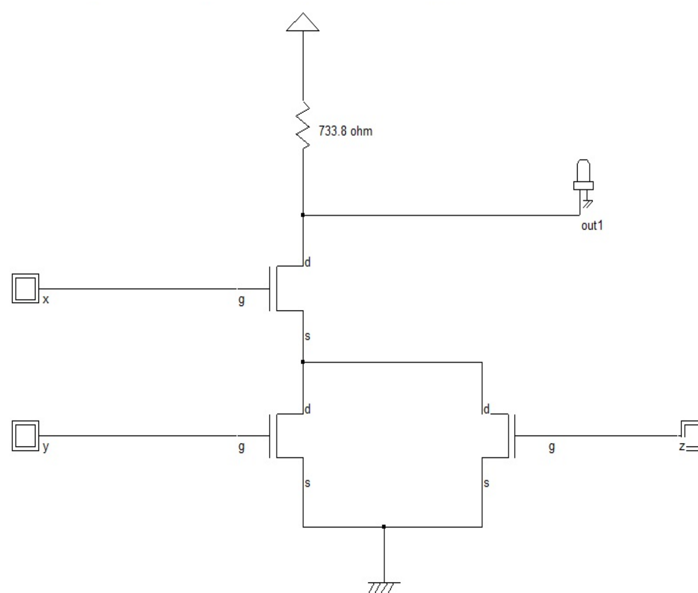


Figure 5. Three inputs resistive loaded nano-MOSFET complex logic circuit

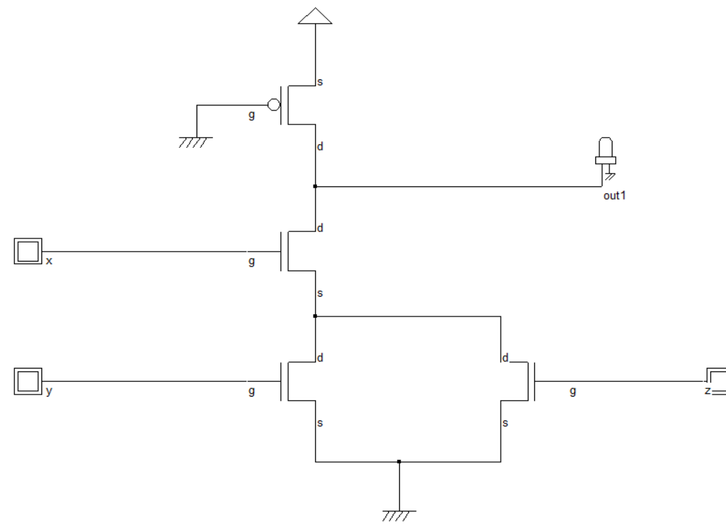
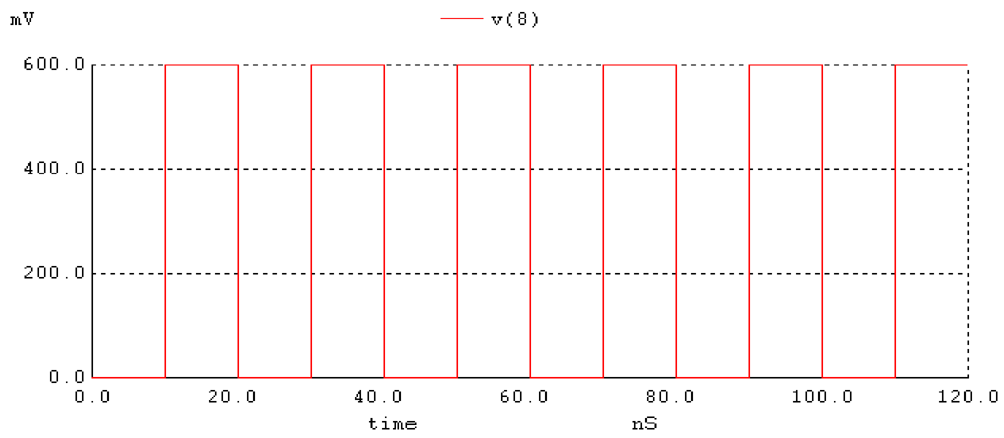
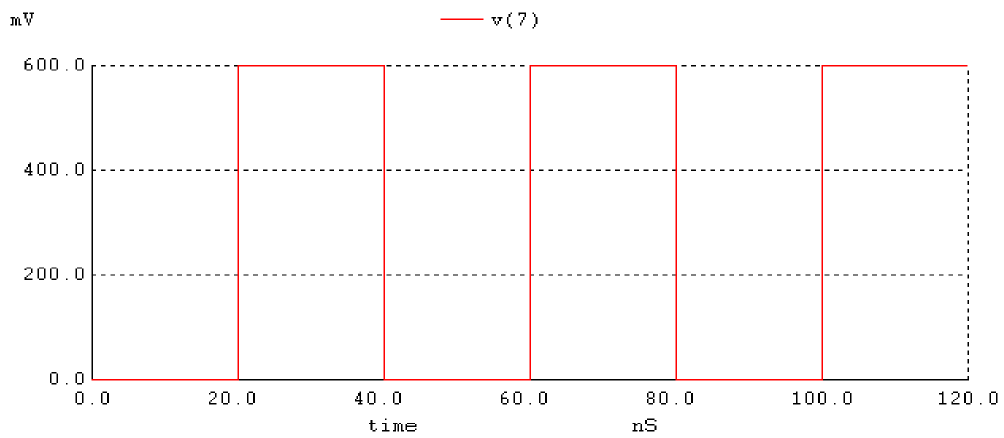


Figure 6. Three inputs pseudo n-type nano-MOSFET complex logic circuit

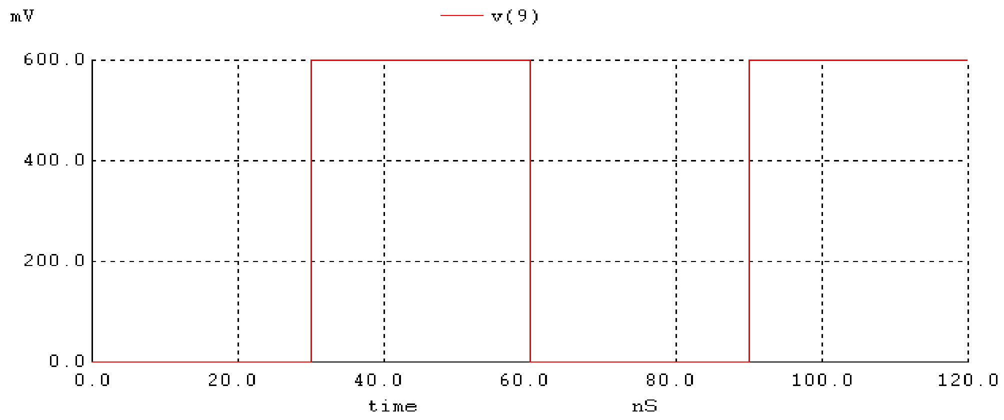
The three input signals to circuits in Figures 3-6 are shown in Figure 7. All these three input signals have 50% duty cycle and amplitude of 0.6 V.



(a) First input signal



(b) Second input signal



(c) Third input signal

Figure 7. Input signals to all four complex logic circuits

The output signals of circuits in Figure 3, Figure 4, Figure 5 and Figure 6 are shown in Figure 8, Figure 9, Figure 10 and Figure 11, respectively. These output waveforms showed correct complex logical Boolean expression $\overline{x(y+z)}$ with inputs as in Table 3.

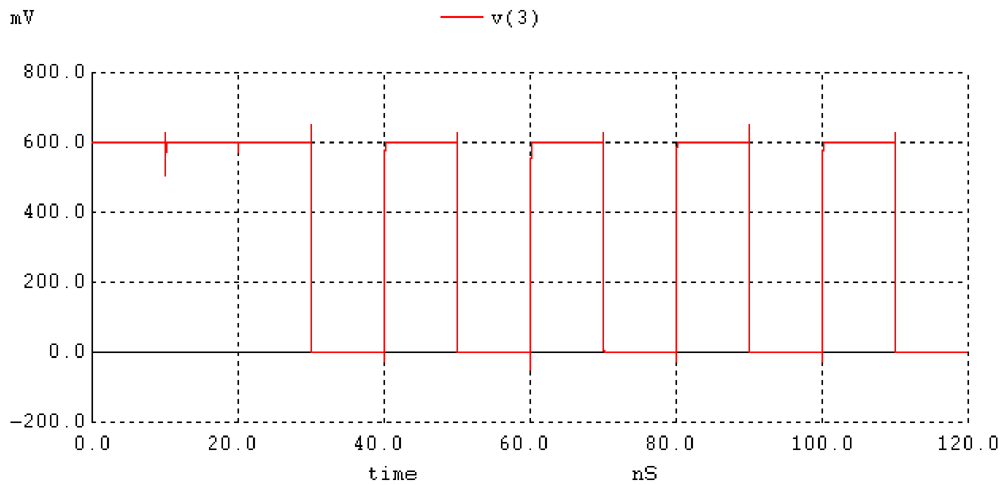


Figure 8. Output signal of nano-CMOS complex logic circuit

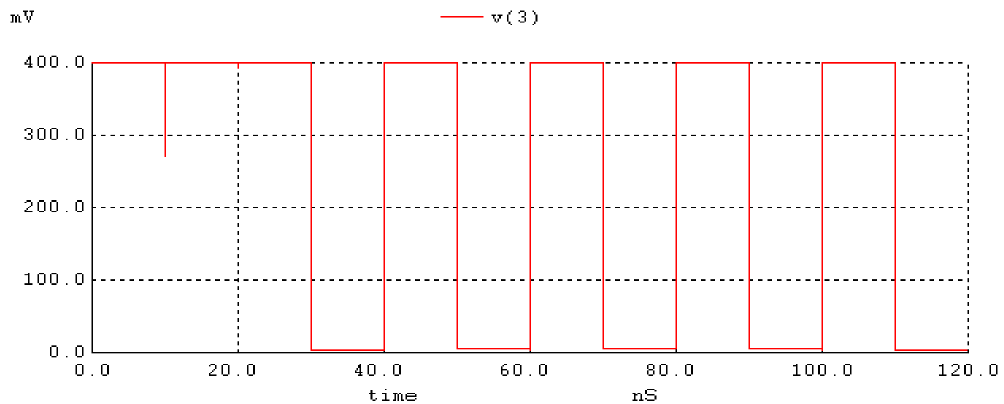


Figure 9. Output signal of nano-MOSFET loaded nano-MOSFET complex logic circuit

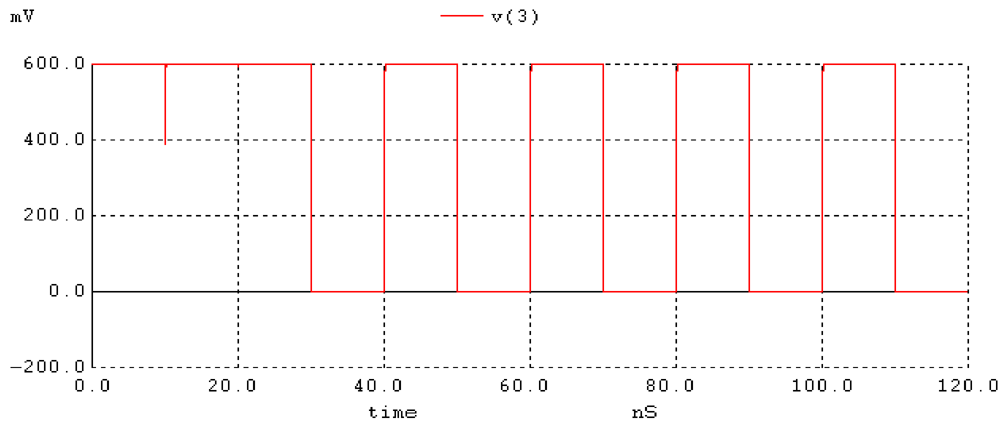


Figure 10. Output signal of resistive loaded nano-MOSFET complex logic circuit

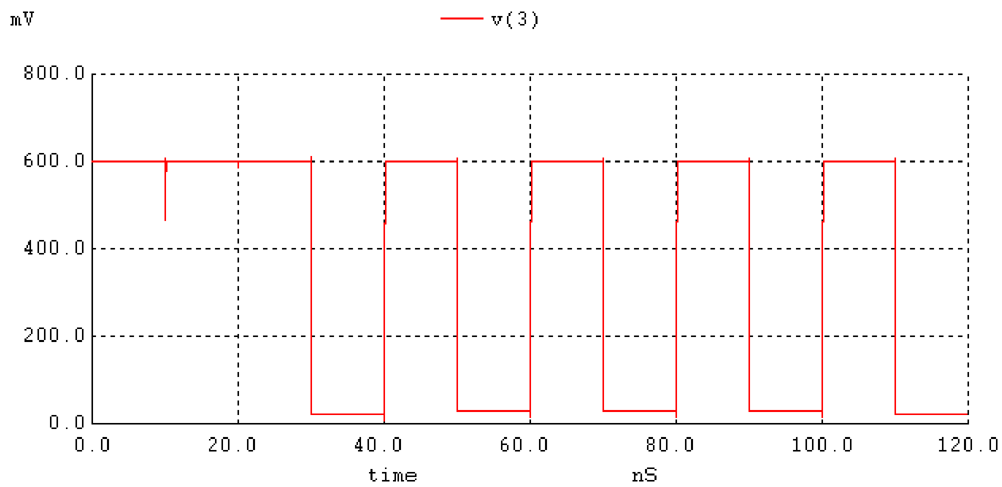


Figure 11. Output signal of pseudo n-type nano-MOSFET complex logic circuit

Figure 9 is the output signal of logic circuit in Figure 4, with an amplitude of 0.4 V due to the threshold voltage loss of 0.2 V at the load nano-MOSFET which acts as n-type pass transistor [24-25]. The output signal of logic circuit in Figure 5 has an amplitude of 0.6 V as shown in Figure 10. The pseudo n-type nano-MOSFET logic gate has p-type nano-MOSFET with L = 10 nm and W = 125 nm whereas n-type nano-MOSFET with L = 10 nm and W = 250 nm. To reduce the output low voltage, V_{OL}, the criteria $\left(\frac{W}{L}\right)_n \geq 2\left(\frac{W}{L}\right)_{Load}$ must be fulfilled. The output signal of the logic circuit in Figure 6 as shown in Figure 11, shows that the output is not 0 when compared with other output waveforms because pseudo PMOS is always ON and current still flow during output low state and thereby caused small output voltage during logic 0 state.

Figure 12 shows the transient analysis output signal for logic gate in Figure 4. Rise time and fall time are taken between 10% to 90% and 90% to 10% of output voltage signal at rising edge and falling edge, respectively. Rise time is due to charging circuit whereas fall time is due to discharging circuit. The simulated fall time is 0.692 ps and rise time is 2.69 ps with period of 120 ps which is equivalent to pulse width of 70 ps (58.33% duty cycle). The theoretical calculated propagation delay is 0.0346 ps as tabulated in Table 2, whereas the simulated propagation delay is 0.180 ps as measured from WinSpice output result. Therefore, the theoretical switching speed is 5.22 times faster than the simulated value. From Table 2 and Table 4, the theoretical maximum frequency of operation is around 758 GHz whereas the simulated maximum frequency of operation is 295 GHz, with 61% percentage error. The difference in both results occurs as quasi-ballistic transport model is used whereas in the WinSpice simulation, quantum corrected drift-diffusion model is used. Scattering events are more obvious in quantum corrected drift-diffusion model than the quasi-ballistic transport model. Therefore, the theoretical quasi-ballistic model has a shorter delay and hence a faster frequency. Thus, a high speed complex logic gate designed with nano-MOSFET has been achieved. From [11], the propagation delays of 45 nm MOSFET logic gates typically has value of 8.72 ps. When compared with the theoretical and simulated propagation delays which are 0.0346 ps and 0.180 ps, respectively as reported in this paper, complex logic gates designed by 10 nm nano-MOSFET have a faster speed. Therefore, downscaling nano-MOSFET has led to faster speed of logic circuits [10]. From Figure 12, the simulated output low voltage V_{OL} is 5 mV whereas the theoretical calculated value of V_{OL} is 53.88 mV as derived from Equation (14) in Section 2 [26]. Table 4 tabulates WinSpice simulated timing characteristic.

Table 4. Simulated value timing characteristics of three inputs complex logic gate

WinSpice Simulation Results Using Model Level MOS6 (10% and 90% Points)				
Logic Gates	Rise Time (t_r)	Fall Time (t_f)	Propagation Delay (t_p)	Maximum Operating Frequency (f_{max})
Complex	2.69 x 10^{-12} s	69.23 x 10^{-14} s	1.80 x 10^{-13} s	2.95 x 10^{11} Hz

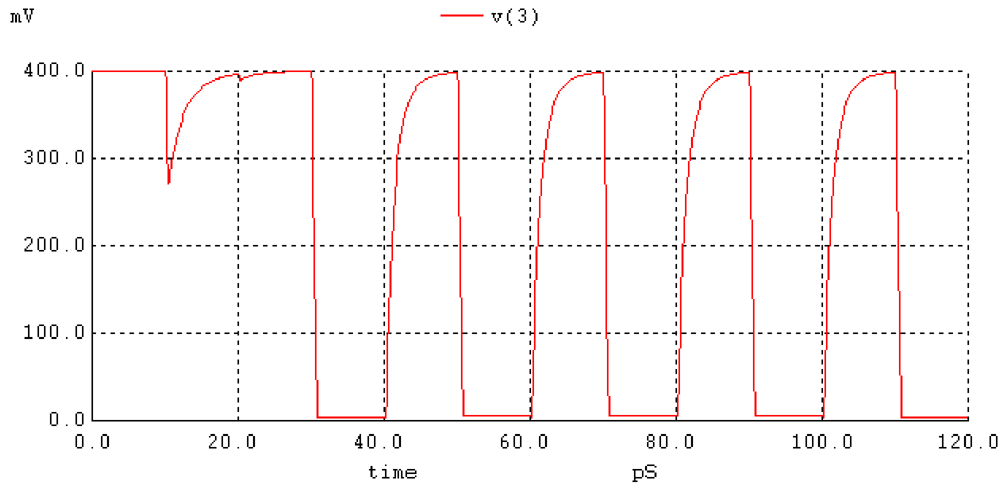


Figure 12. Transient output signal of nano-MOSFET loaded nano-MOSFET complex logic circuit

Table 5. Power dissipation of three inputs complex logic gate

	Nano-CMOS Complex	Nano-MOSFET Loaded Complex	Resistive Loaded Complex	Pseudo Nano-MOSFET Complex
Dynamic power (Watts)	5.827 x 10^{-7}	2.826 x 10^{-7}	1.942 x 10^{-7}	3.884 x 10^{-7}
Voltage supply (Volts)	0.6	0.6	0.6	0.6
Frequency of switching (Hertz)	5 x 10^{11}	5 x 10^{11}	5 x 10^{11}	5 x 10^{11}

Simulated fall time value is about 174 times than that of theoretical value because in simulation analysis quantum corrected drift-diffusion transport is used where scattering events cannot be ignored. Since there are many capacitance in the discharging circuit, simulated fall time are larger than theoretical fall time which used quasi-ballistic transport. Moreover, from [19], propagation delay of logic gate with W = 1 µm, L = 120 nm, T_{Si} = 60 nm MOSFET is 3.534 ps. When compared with simulated 0.180 ps, there is an improvement of 20 times in speed in 10 nm nano-MOSFET complex logic circuits.

Table 5 tabulates the power dissipation for four different complex logic gates with Boolean expression $\overline{x(y+z)}$ calculated using Equation (15) in Section 2 with a = 0.234375. When compared with the logic gate designed using MOSFET with W = 1 µm, L = 120 nm and T_{Si} = 60 nm, which has a downscaled power dissipation of 140.9 µW range as reported in [19], all four logic families complex gates show power reduction during downscaling of nano-MOSFET to nano-meter regime.

The power reduction for nano-CMOS, nano-MOSFET loaded, resistive loaded and pseudo nano-MOSFET complex logic circuits are 241, 498, 725 and 362, respectively when benchmarked against [19]. The nano-CMOS complex logic circuit showed the highest power dissipation because the number of switching nano-MOSFETs is the highest followed by pseudo nano-MOSFET complex logic circuit which can save two nano-MOSFETs when compared to nano-CMOS complex logic. The power dissipation of pseudo nano-MOSFET complex logic circuit is the second highest because the pseudo PMOS is always ON. The third highest power dissipation complex logic circuit is the nano-MOSFET loaded complex logic circuit because there is a small voltage drop across the load pass transistor. The lowest power dissipation complex logic circuit is the resistive loaded complex logic circuit because the load is purely resistive.

4. CONCLUSION

In this paper, nano-MOSFETs have been investigated through simulation to be used in designing logical three inputs complex logic circuits with Boolean expression $\overline{x(y+z)}$. Besides having a correct complex logical operation as stated in the truth table, all four complex logic families circuits designed have the characteristics of low power dissipation and high speed. These low power high speed nano-MOSFET complex logic circuits are suitable in modern consumer electronics products which needs to process large amount of data quickly and have long batteries life.

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